Thermal HALT - a tool for discovery Signal Integrity and Software reliability issues

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The differential voltage, the “eye” in the eye diagram is shrinking as clock and bus frequencies increase.

Undistorted eye diagram of band limited signal

Eye diagram of signal with amplitude (noise) and phase (timing) errors

From “Analyzing Signals Using the Eye Diagram” November 2005 High Frequency Electronics
Little data exist on relationship of PWBA hardware variations and effects on signal integrity and software failures at

Affects in data transmission that were 2\textsuperscript{nd} or 3\textsuperscript{rd} order in previous designs begin to dominate as bus speeds increase

– Not a big deal before, become a big deal in SI
– Many new variables that are difficult to model correctly
– Decrease in IC metallization an higher frequency’s will result in higher sensitivity to fabrication variations
No Fault Found (NFF) Field Returns

Many causes for warranty returns that are NFF

Some Intermittent failures due to low SI margin

Signal Integrity operational margin due to voltage, board impedance, crosstalk, noise, etc
Many companies do not consider it a “failure”

- no root cause investigation
- may be returned to field or as a replacement part for repair depot
- Marginal operation may be less in another system – Ex. graphics cards, or DIMMs (DRAM memory)
Signal Integrity (SI) and HALT

SI operational issues may significantly contribute to NFF

Very difficult to observe in the field and on a test bench

- May take hundreds of operational cycles to observe
- Marginality may only occur in the stack up of a specific whole system hardware
- NFF when tested on bench or in the “golden” system
Using Thermal Stress for Timing variations

• Thermal Stress is very useful for stimulation of timing variations—Both high and **Low** temperature limits

  – High temperature – lower speed

  – Low temperature – higher speed
Effect of Temperature on Signal Propagation

Measured low-to-high propagation delay versus case temperature in Fairchild Octal buffer MM74HC244N (rated for -40 to 85C)

Thermal stress provides stimulation of signal propagation variation.
Lot to Lot Variation of Signal Propagation?

Predicting the Future variations

• How much propagation variation die to die, and lot to lot?
• How close to the specified maximum delay?
• How will variation impact operational reliability in each in-circuit application of the component?
Temperature can skew signal propagation IC’s and conductors.
Timing and quality of SI variations come from:

- Lot to lot manufacturing
- Within lots
- Board impedance variations
- Second and third source components
- Interconnects
- Parametric drift - Aging
**Signal Integrity**

- Electric and Magnetic fields - noise, crosstalk, reflections
- Every conductor - frequency dependant Inductance, Capacitance and resistance impacts the quality of signal transmissions from each node of the non-ideal conductor
- Surface on Copper affects L and R – rough for FR4 adhesion

![Typical transmission lines in PCB cross section](image)

Referenced from S.H. HALL and H.L. Howard, "Advanced Signal Integrity for High-Speed Designs", Wiley and Sons, 2009
Marginal designs may not be discovered until a sufficient number of units are in the field.

Field - costly place to discover these marginal conditions or have high NDF returns if not discovered.
Applying thermal stress stimulates a timing shift

- Thermal Step Stress skews the signal propagation speeds in components and assemblies
- Rapid thermal transitions provide higher thermal gradients across components and PWBA – mix of parametrics skewing
Fiber weave effect - *weave of dielectric cannot be assumed homogeneous at Gb/s transmission rates*

RH (relative humidity) has an impact on the electrical performance of the dielectric – *dramatic increase of insertion loss from dry Arizona to humid Malaysia*

**Signal Integrity**

Typical transmission lines in PCB cross section

Referenced from S.H. HALL and H.L. Howard, "Advanced Signal Integrity for High-Speed Designs", Wiley and Sons, 2009
Thermal stress expands and contracts material dimensions

Heat expands materials, dimensions
Thermal stimulation for Signal Integrity Margin

Can provide stimulation of potential affects and impact of variation of parametrics, noise, L, C, R resulting from manufacturing, materials variation

Cooling contracts materials, dimensions
Thermal cycling adds an additional variation – thermal gradients create differential parametric shift from shifts in dimensions and impedance.

Thermal Gradients provide differential mechanical and parametric stresses.
No Fault Found (NFF) Field Returns

Two computers returned from two different customers with same reported intermittent failure condition

- After five days of bench testing, OEM Failure Analysis could not duplicate the failure mode
- Units were declared NFF
- Same units placed in thermal cycling (+65 to -10 °C) reproduced the same (soft) failure mode as reported by the customer 3 times in a 24 hour period
Combined HALT Stress Interactions

Stresses combinations can have significant interactions for multi-dimensional limit or boundary maps

Clock/bus Frequency margining limits

Voltage margining limits
Stress Boundary Maps

distributions in the boundary identifies reliability margin risks

HALT Operational Limit

“Four Corner” test points

Derating boundary 5% guard band

Normal user operating ranges

Clock/bus Frequency

temperature

voltage
Wide distributions in limits – higher risk of stress strength overlap
First Presented at the IEEE/CPMT 2010 ASTR Workshop

- **Donovan Johnson**
  Senior Hardware & Reliability Test Engineer
- **Ken Franks**
  Hardware & Reliability Test Manager
2004 Gregg Hobbs, Ph.D. gave a “Mastering HALT and HASS” Class at New Zealand research and development centre

The term “software fault” is defined at Allied Telesis (formerly Allied Telesyn) as a fault found in:

- The firmware of a product, such as code in a Programmable Logic Device (PLD)
- The boot code of a product, such as EPROM boot code.
- The operating system of a product.
Test at each thermal step during HALT

- External traffic test – use industry standard equipment
- Power Cycling – margin voltage and frequency
- Internal memory test – RAM and NVS testing
- Internal packet generator test – CPU, Encryption engine and RAM test
- Other product specific tests
Nearly one-third of the issues found in HALT were software related.

- Cold spray to cool component
- Power resistors used to heat component
Failure Types Found in HALT

**FAILURE PERCENTAGE**

- **Hardware issues**: 70%
- **Software issues**: 28%
- **To be determine**: 2%

Software issues: 28%

Hardware issues: 70%

To be determined: 2%
Abnormal LED Activity

• This anomaly was found during cold step testing at minus 10°C and attributed to the reset pulse timing inside PLD code.

• After change to PLD code the system operated to -50°C.
Switch Tuning

- Change in UOL from 70°C to greater than 100°C and LOL from minus 20 to less than minus 60°C.

Changes in software increase operational temperature range of 90°C to 160°C.
Software Issues found using HALT

System Crash

• A product that had been in the field for six months
• First HALT the UOL of 70°C – failure was a system crash
• Changed register setting inside the boot code allowed operation to 100°C.
• In addition to the software fault, a flaw within the CPU silicon was revealed, which amplified the effects of the software fault.
Software Issues found using HALT

System Silent Reboot

• Rapid Thermal Transitions exposed a flaw in software during temperature ramps even though the initial failure occurred in a moderate climate inside a server room.

• Failure mode was only apparent when running one particular test. A software patch fixed this problem.
Silent Reboot

- The same fault took weeks to replicate intermittently using traditional methods.
- The same failure mode was repeatedly replicated in HALT in less than one day of testing.
Thermal HALT has multiple benefits in electronics systems testing

- Well established for hardware latent defects

- Secondary and less recognized (Opportunity) – Thermal induced skewing of signal speeds in components and PWB assemblies help to discover marginal SI that may result in failures of software and firmware.
The material in this presentation is contained in our new book *Next Generation HALT and HASS: Robust Design of Electronics and Systems* published by John Wiley & Sons, June, 2016

Co-Authored with John J. Paschkewitz